

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Rosenberg et al.

Application No: 08/993,104

Filed: December 18, 1997

For: VOLTAGE SIGNAL
MODULATION SCHEME



Examiner: Not Yet Assigned

Art Unit: 2871

Assistant Commissioner for Patents
Washington, DC 20231
BOX: ISSUE FEE

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Transmitted herewith is a complete set of formal drawings, comprising seven (7) sheets and seven (7) figures for the above-identified application.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 3-17, 1999

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Date

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

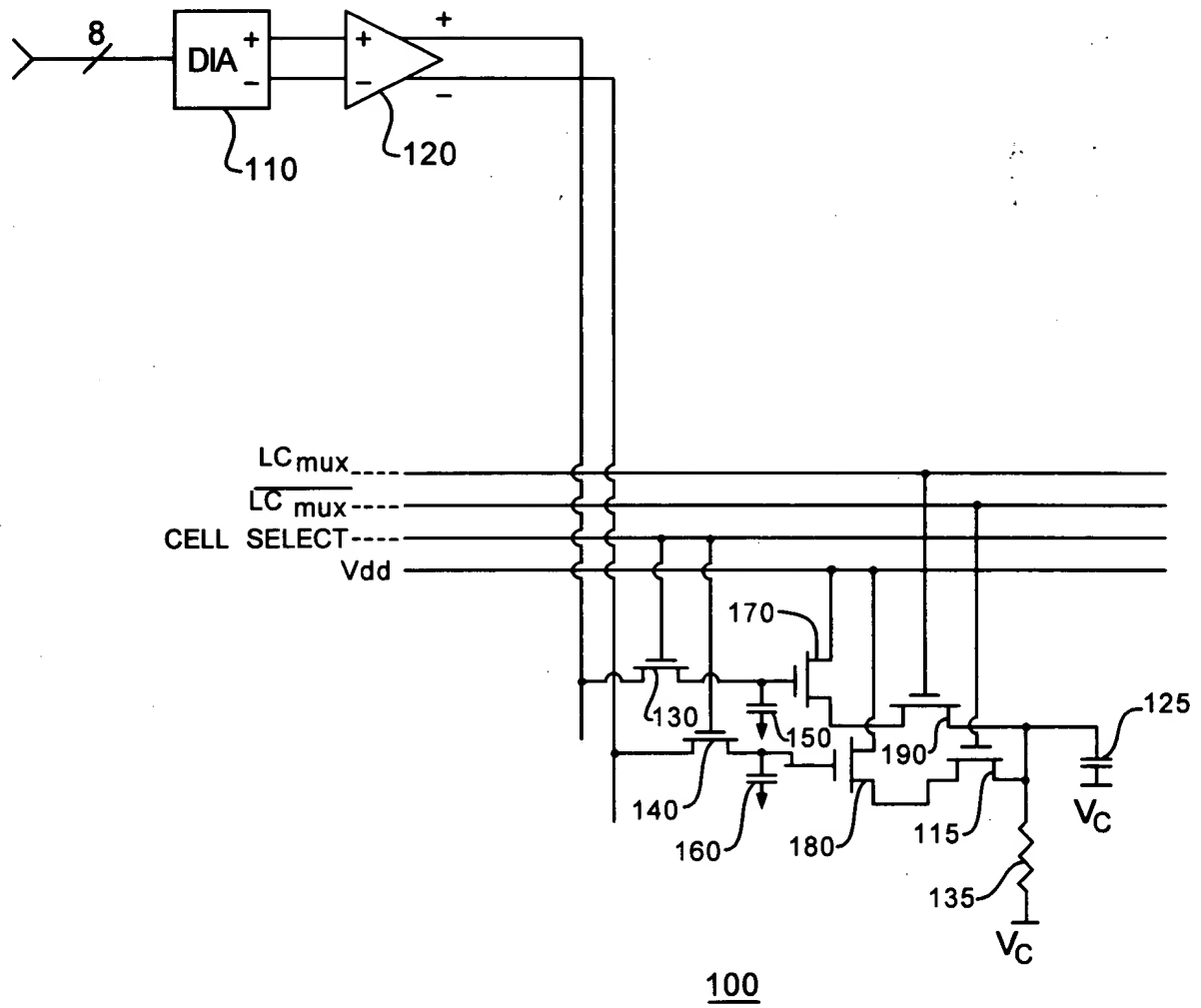


FIG. 1

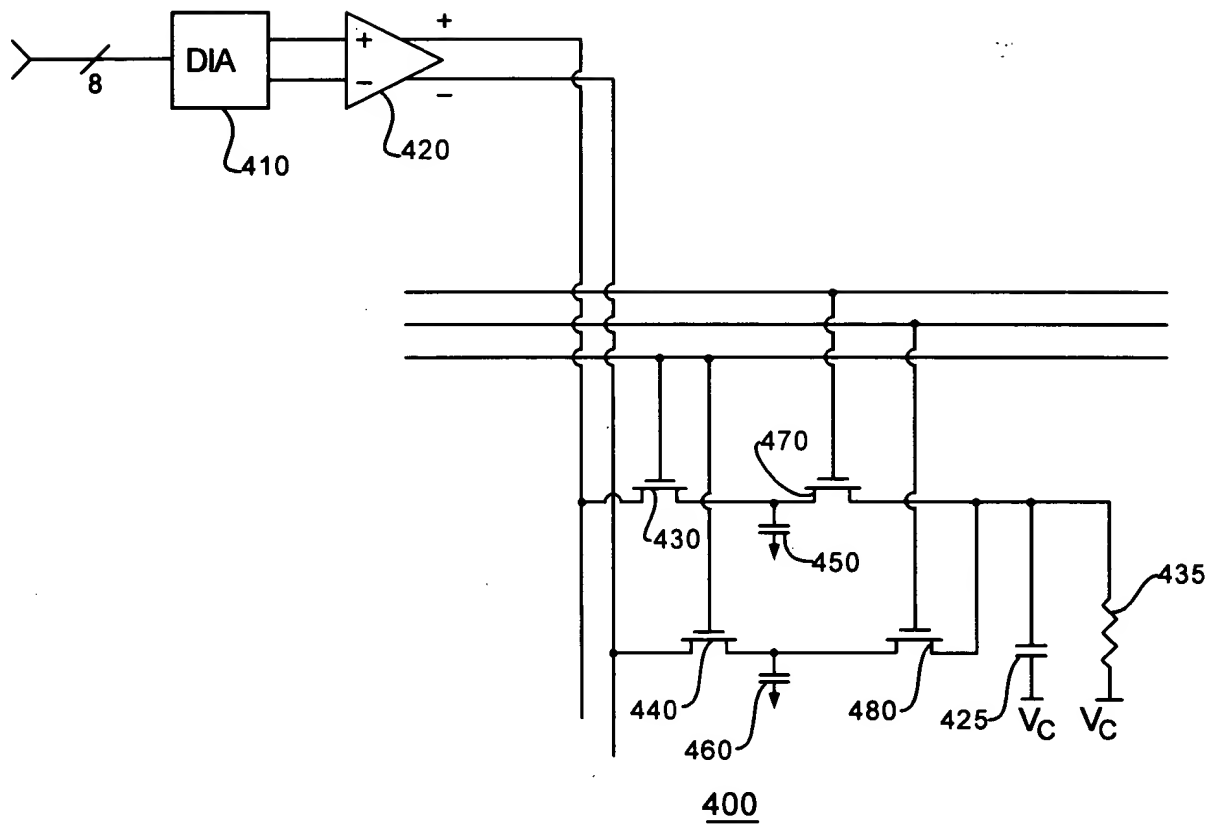
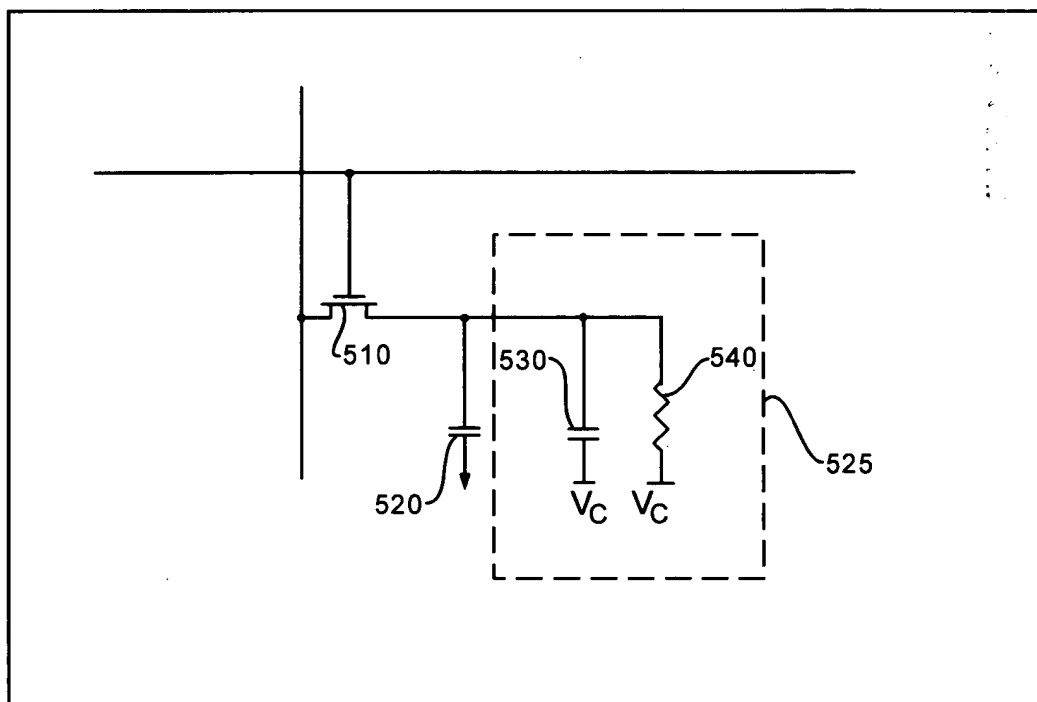


FIG. 3



INTEGRATED
CIRCUIT (IC)
CHIP

500

FIG. 4

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

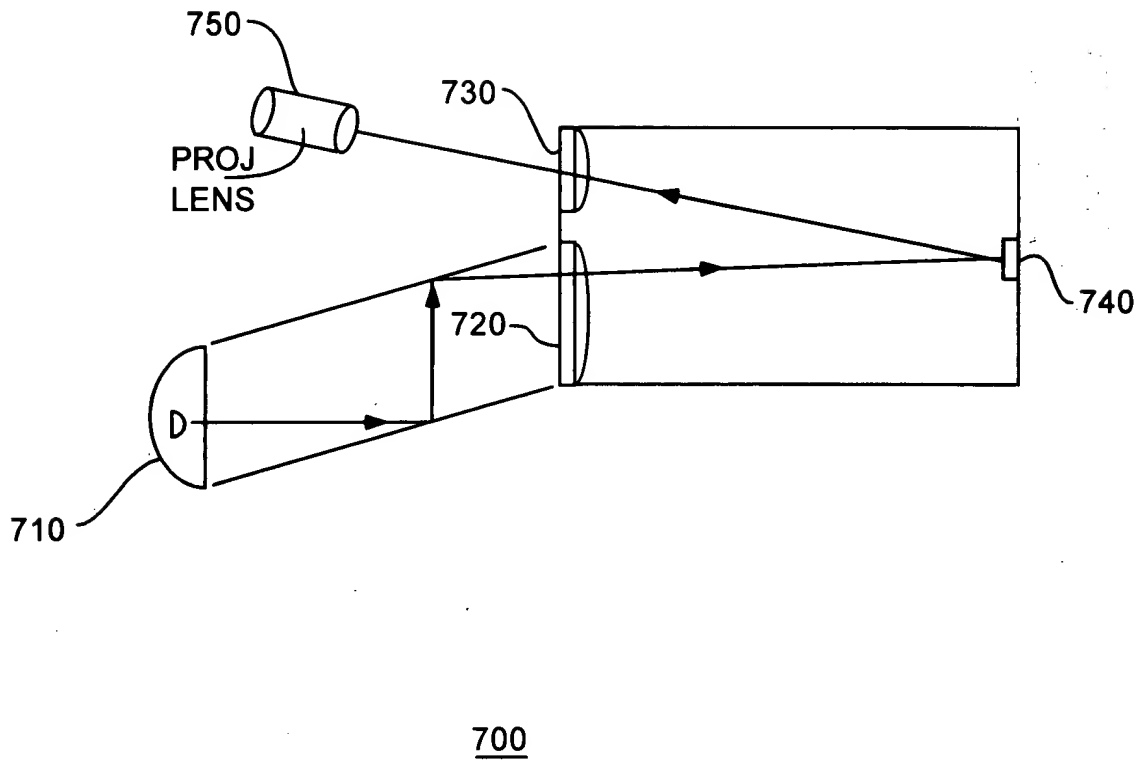
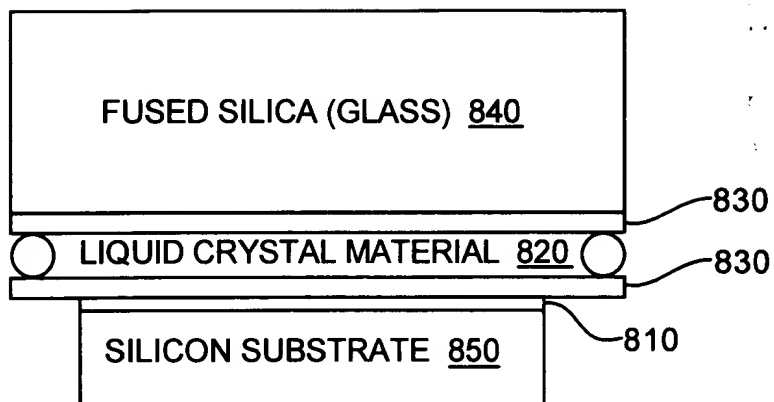


FIG. 5

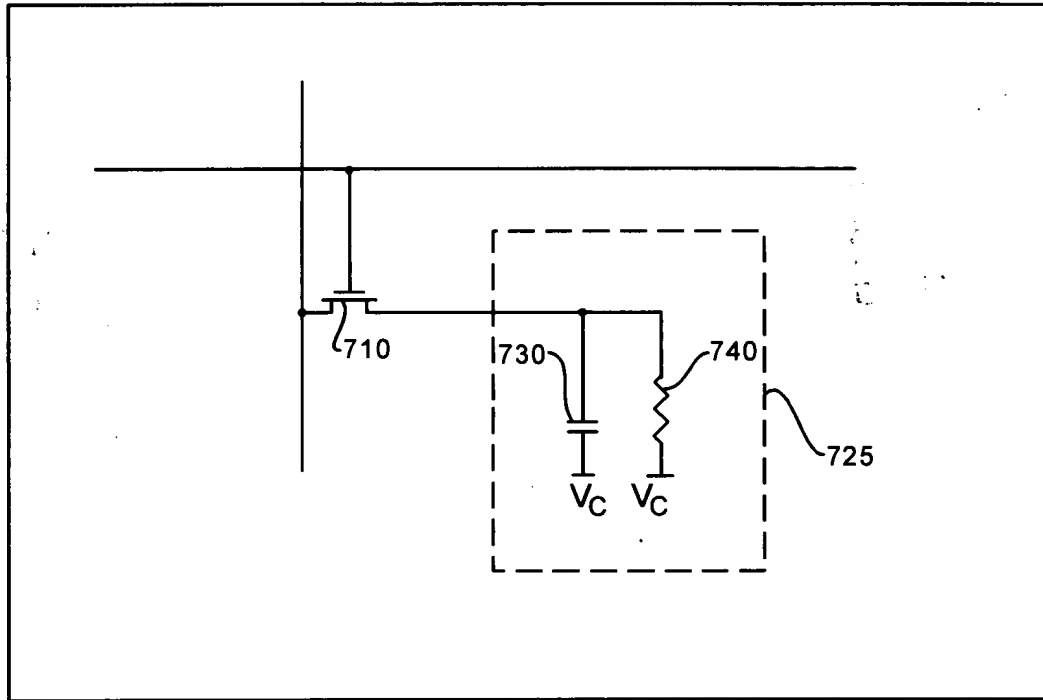
APPROVED	O.G. FIG.	
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800

FIG. 6

APPROVED	O.G. FIG.	
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INTEGRATED
CIRCUIT (IC)
CHIP

700

FIG. 7